

## Refine Search

### Search Results -

Terms	Documents
L1 and (switch\$3 near10 node)	1

**Database:**

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US OCR Full-Text Database  
EPO Abstracts Database  
JPO Abstracts Database  
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IBM Technical Disclosure Bulletins

**Search:**

L2	<input type="button" value="Refine Search"/>
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### Search History

**DATE:** Wednesday, May 17, 2006 [Printable Copy](#) [Create Case](#)**Set Name Query**

side by side

DB=PGPB; PLUR=YES; OP=OR

L2 L1 and (switch\$3 near10 node)L1 "memory hub" same control\$3 same (request\$3 or command\$3)**Hit Count Set Name**

result set

1 L257 L1

END OF SEARCH HISTORY

## Refine Search

### Search Results -

Terms	Documents
L1 and (switch\$3 same node)	1

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**Search:**

L3

### Search History

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side by side

*DB=PGPB; PLUR=YES; OP=OR*

	<b>Hit Count</b>	<b>Set Name</b>
<u>L3</u> L1 and (switch\$3 same node)	1	<u>L3</u>
<u>L2</u> L1 and (switch\$3 near10 node)	1	<u>L2</u>
<u>L1</u> "memory hub" same control\$3 same (request\$3 or command\$3)	57	<u>L1</u>

END OF SEARCH HISTORY

## Refine Search

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### Search Results -

Terms	Documents
"memory hub" same control\$3 same (request\$3 or command\$3)	69

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Recall Text

Clear

Interrupt

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### Search History

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*DB=PGPB,USPT,USOC; PLUR=YES; OP=OR*

L4 "memory hub" same control\$3 same (request\$3 or command\$3)

*DB=PGPB; PLUR=YES; OP=OR*

L3 L1 and (switch\$3 same node)

L2 L1 and (switch\$3 near10 node)

L1 "memory hub" same control\$3 same (request\$3 or command\$3)

**Hit Count Set Name**

result set

69 L4

1 L3

1 L2

57 L1

END OF SEARCH HISTORY

## Refine Search

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### Search Results -

Terms	Documents
"memory hub" same control\$3 same (request\$3 or command\$3)	11

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**Database:**

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**Search:**

Refine Search

Recall Text

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---

### Search History

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DATE: Wednesday, May 17, 2006 [Printable Copy](#) [Create Case](#)

**Set Name Query**

side by side

**Hit Count Set Name**  
result set

*DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR*

L5 "memory hub" same control\$3 same (request\$3 or command\$3) 11 L5

*DB=PGPB,USPT,USOC; PLUR=YES; OP=OR*

L4 "memory hub" same control\$3 same (request\$3 or command\$3) 69 L4

*DB=PGPB; PLUR=YES; OP=OR*

L3 L1 and (switch\$3 same node) 1 L3

L2 L1 and (switch\$3 near10 node) 1 L2

L1 "memory hub" same control\$3 same (request\$3 or command\$3) 57 L1

END OF SEARCH HISTORY

## Refine Search

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### Search Results -

Terms	Documents
(709/201  709/219  361/679  361/684  345/418  710/100  710/300  710/104  710/311  710/5  710/303  710/2  710/305  710/316  370/351  370/338  370/423  370/912  711/105  711/119  711/149  711/5  711/154  712/11  712/15  712/34  712/220  713/400  365/63  365/52  365/230.01).ccls.	28221

<b>Database:</b>	<input type="checkbox"/> US Pre-Grant Publication Full-Text Database <input type="checkbox"/> US Patents Full-Text Database <input type="checkbox"/> US OCR Full-Text Database  <input type="checkbox"/> EPO Abstracts Database <input type="checkbox"/> JPO Abstracts Database <input type="checkbox"/> Derwent World Patents Index <input type="checkbox"/> IBM Technical Disclosure Bulletins
<b>Search:</b>	L6 <div style="float: right; margin-top: -20px;"> <input type="button" value="Refine Search"/> </div>
<input type="button" value="Recall Text"/> <input type="button" value="Clear"/> <input type="button" value="Interrupt"/>	

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### Search History

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DATE: Wednesday, May 17, 2006    [Printable Copy](#)    [Create Case](#)

Set

Name Query

side by  
side

*DB=PGPB,USPT,USOC; PLUR=YES; OP=OR*

L6 710/100,300,104,311,5,303,2,305,316;712/11,15,34,220;365/63,52,230.01;361/679,684;345/418;370/351,338,42

*DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR*

L5 "memory hub" same control\$3 same (request\$3 or command\$3)

*DB=PGPB,USPT,USOC; PLUR=YES; OP=OR*

L4 "memory hub" same control\$3 same (request\$3 or command\$3)

*DB=PGPB; PLUR=YES; OP=OR*

L3 L1 and (switch\$3 same node)

L2 L1 and (switch\$3 near10 node)

L1 "memory hub" same control\$3 same (request\$3 or command\$3)

END OF SEARCH HISTORY

## Refine Search

### Search Results -

Terms	Documents
L1 and L6	27

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### Search History

**DATE: Wednesday, May 17, 2006** [Printable Copy](#) [Create Case](#)[Set](#)[Name Query](#)[side by side](#)*DB=PGPB,USPT,USOC; PLUR=YES; OP=OR*L7 11 and L6L6 710/100,300,104,311,5,303,2,305,316;712/11,15,34,220;365/63,52,230.01;361/679,684;345/418;370/351,338,42*DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR*L5 "memory hub" same control\$3 same (request\$3 or command\$3)*DB=PGPB,USPT,USOC; PLUR=YES; OP=OR*L4 "memory hub" same control\$3 same (request\$3 or command\$3)*DB=PGPB; PLUR=YES; OP=OR*L3 L1 and (switch\$3 same node)L2 L1 and (switch\$3 near10 node)L1 "memory hub" same control\$3 same (request\$3 or command\$3)**END OF SEARCH HISTORY**

# EAST - [Untitled1:1]

File View Edit Tools Window Help

-  X  
-

Drafts

Pending

Active

L1: (12) "memory hub"

Failed

Saved

Favorites

Tagged (0)

UDC

Queue

Trash

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DBs USPA

Default operator: OR

Plots

Highlight all hits manually

OR

AND

NOT

NEAR

WITHIN

REGEXP

WORD

PHRASE

NEAR

WITHIN

EAST - [Untitled1:1]

 File View Edit Tools Window Help



- ✉ Drafts
- ⌚ Pending
- 🕒 Active
  - ⌚ 11: (12) "memory hub"
- ✉ Failed
- ✉ Saved
- ✉ Favorites
- ⌚ Tagged (0)
- ⌚ UDC
- ⌚ Queue
- ⌚ Trash

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CS3      USPAT

Default operator: OR       Plurals       Highlight all hit terms initially

```
"memory hub" same control$3 same (request$3 or command$3)
```

 BPS form  S&R form  Image  Text  HTML

U	I	Document ID	Issue Date	Pages	Title	Current OR	Current X
1	✓	US 7047351	20060516	11	Memory hub bypass circuit and method	711/5	365/230.0
		B2				:	:
2	✓	US 7035212	20060425	22	Method and apparatus for end to end forwarding	370/230	370/413;
		B1				711/202	
3	✓	US 6980042	20051227	19	Delay line synchronizer apparatus and method	327/291	327/141;
		B2				327/160;	
4	✓	US 6877052	20050405	8	System and method for improved half-duplex bus	710/107	710/105;
		B1				710/240;	
5	✓	US 6865192	20050308	9	Integrated services hub self-configuration	370/475	710/104
		B1					
6	✓	US 6820181	20041116	14	Method and system for controlling memory access	711/169	710/52
		B2					
7	✓	US 6754117	20040622	14	System and method for self-testing and repair	365/201	365/200
		B2					
8	✓	US 5461627	19951024	19	Access protocol for a common channel wireless	370/346	370/349
		A					
9	✓	US 4253146	19810224	82	Module for coupling computer-processors	709/226	711/147;
		A				711/150	
10	✓	US 4253144	19810224	84	Multi-processor communication network	709/226	711/147;
		A				711/150	
11	✓	US 4245306	19810113	83	Selection of addressed	709/245	709/233;

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( (memory hub) and control\* and switch\*&lt;in&gt;metadata )

 Check to search only within this results set[» Key](#)Display Format:  Citation  Citation & Abstract

IEEE JNL IEEE Journal or Magazine

IEE JNL IEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

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IEEE STD IEEE Standard

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**Key**

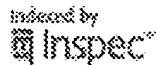
IEEE JNL	IEEE Journal or Magazine
IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

**1. Design and packaging challenges for on-board cache subsystems using source synchronous 400 Mb/s Interfaces**

Nam Pham; Cases, M.; Guertin, D.;  
[Electronic Components and Technology Conference, 2001. Proceedings, 51st](#)  
29 May-1 June 2001 Page(s):123 - 127  
Digital Object Identifier 10.1109/ECTC.2001.927706  
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## Design and packaging challenges for on-board cache subsystems using source synchronous 400 Mb/s interfaces

Nam Pham Cases, M., Guertin, D.

eServer X Series, IBM Corp., Austin, TX, USA;

This paper appears in: [Electronic Components and Technology Conference, 2001. Proceedings... 51st](#)

Publication Date: 29 May-1 June 2001

On page(s): 123 - 127

Number of Pages: xxxiii+1518

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Location: Orlando, FL

INSPEC Accession Number:7049073

Digital Object Identifier: 10.1109/ECTC.2001.927706

Posted online: 2002-08-07 00:28:18.0

**Abstract**

This paper describes circuit and packaging design challenges encountered while attempting to optimize the source synchronous timing equations for the system level interconnects using a 200 MHz double data rate (DDR) level 3 (L3) cache subsystem. Various solutions to these challenges are presented. The delay skew budget and noise margin allocation for the various components of the optimization equations are discussed in conjunction with their associated delay skew control techniques

**Index Terms**

Inspec

**Controlled Indexing**

cache storage integrated circuit design integrated circuit interconnections microprocessor chips packaging

**Non-controlled Indexing**

200 MHz delay skew design optimization microprocessor circuit noise margin on-board DDR level 3 cache subsystem packaging source synchronous interface system-level interconnect timing allocation

**Author Keywords**

Not Available

**References**

No references available on IEEE Xplore.

**Citing Documents**

- 1 Statistical signal integrity analysis and diagnosis methodology for high-speed systems, Matoglu, E.; Pham, N.; de Araujo, D.N.; Cases, M.; Swaminathan, M.

*Advanced Packaging, IEEE Transactions on [see also Components, Packaging and Manufacturing Technology, Part B: Advanced Packaging, IEEE Transactions on]*

On page(s): 611- 629, Volume: 27, Issue: 4, Nov. 2004

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